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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/007,904	10/31/2001	H. Scott Fetterman	7-17	3045

7590 02/25/2003

Docket Administrator
Agere Systems Inc.
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EXAMINER	
PERT, EVAN T	
ART UNIT	PAPER NUMBER
2829	

DATE MAILED: 02/25/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/007,904	Applicant(s) FETTERMAN ET AL.	
	Examiner Evan T. Pert	Art Unit 2829	

-- The MAILING DATE of this communication appears on the cover sh et with th correspond nce address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 November 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-41* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-41* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 August 2002* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *2* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Election/Restrictions

1. Applicant's election with traverse of claims 1-33 in Paper No. 5 is acknowledged. The traversal is on the grounds that "only a single invention is present" [p. 2] and that "the examiner has not established a *prima facie* case that the invention as claimed in claims 1-33 (invention I) can be used in a materially different process than the claimed process" [p. 1]. While the examiner does not necessarily agree that "one invention is present," the examiner acquiesces to applicant's statement of record and the restriction requirement is therefore withdrawn. Claims 1-41 are pending.

Drawings

2. Figure 10 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-33 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Particularly the terms "test structure" and "test device" render the scope of device claims 1-33 indefinite. A "test" of a "structure" or "device" that will *eventually* form a working part of a functional chip *can* invoke a temporary designation of "test structure" for a part of the chip under construction, in a loose sense. Yet, for purposes of examination, the examiner interprets both "test structure" and "test device" (in the context of the claims and specification) as a dedicated arrangement of conductive runner(s) that do(es) not eventually form a working part of the chip.

In claims 11 and 24, the word "boustrophedonically" is confusing with respect to what further limitation is being recited. This word, not found in a search of the relevant prior art, seemingly most appropriately applies to ancient writing styles (or modern print-head movement) with writing occurring alternatively from right-to-left, then left-to-right, and so forth. Yet, since there is no *clear* reference point for "right" and "left" in a wafer or chip, the examiner interprets "serpentines back and forth boustrophedonically" as being equivalent to "serpentines back and forth in any arbitrary direction(s)."

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1 and 2 are rejected under 35 U.S.C. 102(b) as being anticipated by Bouldin (U.S. 5,514,974).

Bouldin discloses "a wafer" (Fig. 6) with "at least 4 die areas" (e.g. 9 die areas 42 are clearly visible in Fig. 6) thus defining "streets" (depicted in Fig. 6 as spaces delineated between the die 42 as is notoriously well known in the art) wherein "test structures" (monitor and control structures 30/32) are "in a region of two intersecting streets proximate the at least 4 die areas" and these test structures *inherently* form a "stress migration test structure *capable of detecting* stress migration *voids*" [col. 4, lines 1-3].

6. Claims 3, 8, 10-12, 29 and 31 are rejected under 35 U.S.C. 102(b) as being anticipated by Yamamoto (U.S. 5,900,735).

Claim 3 and 29

Yamamoto discloses a stress migration test device comprising: a conductive runner (between A and A' in the cover figure), the runner "having a length sufficient to develop axial stress above the threshold for nucleating voids for the technology in which the runner is fabricated (i.e. > "Blech length"), a plurality of taps (1, 2, 5) along the runner at uniform impedance intervals (3, 4) such that voiding in any segament of the runner "is a detectable portion of the impedance" by passing current between taps 1K and 1A, for example.

Claim 8

The tap conductors 2 are the same line width as the runner (col. 2, lines 60-67).

Claims 10-12 and 31

The runner extends unidirectionally (seen from above in the cover figure), serpentines back and forth (seen as a side view in Fig. 2) and in "on more than one level (also seen in Fig. 2).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 4-7, 9 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamamoto as applied to claims 3 and 29 above, and further in view of Hoang et al. (1991 IEEE article).

Claim 4

Yamamoto is silent about the width of the test structure being "a width that is the minimum line width for the technology in which the runner is fabricated." Yet, Hoang et al. explain that "an understanding of [stress-induced voiding] is important when attempting to use narrow linewidth metallization beneficially." [2nd para., Extended Abstract].

It would have been obvious to one of ordinary skill in the art to choose a test structure for investigating line width effect (e.g. column 1 of Table II), including the minimum possible line width. One of ordinary skill in the art would have been motivated to choose the minimum possible line width since investigating "narrow line width metallization is important" with respect to stress-induced voiding effects.

Claims 5 and 6

Yamamoto is silent about the overall length of the conductive runner being "at least 100 micrometers long" or "at least 400 micrometers long." However, Hoang et al. teach that very long test structures are beneficial for investigating stress-induced voiding (see Table I).

It would have been obvious to one of ordinary skill in the art at the time of the claimed invention to extend the Yamamoto test structure beyond 400 micrometers since this is the shortest length tested for "assessing potential metallization reliability issues early in the technology development phase" [see Table I].

Claim 7

Yamamoto is silent about the length compared to the grain size in the runner, and instead discloses how a minimum length is chosen to assure stress-induced voiding for observation in a test structure.

It would have been obvious to one of ordinary skill in the art at the time of the claimed invention to extend the Yamamoto test structure beyond 400 micrometers as this is the shortest length tested for "assessing potential metallization reliability issues early in the technology development phase" [see Table I].

The length of the runner in Yamamoto when adopting the lengths taught by Hoang et al. (e.g. beyond 400 micrometers per Table I) is inherently longer than 10 crystallographic grains since a grain has an average grain size 2-3 microns (Hoang et al.).

Claims 9 and 30

Yamamoto is silent regarding "two conductive materials providing parallel conduction paths of different impedances," but Hoang et al. explains that such an arrangement is "necessary to carry us into the next generation processes" (last sentence of abstract).

It would have been obvious to one of ordinary skill in the art at the time of the claimed invention to have adopted the well-known Al/TiN interconnect for a "stress-induced voiding test structure" as is taught by Hoang et al., motivated by Hoang et al.'s direction to use "test structures specifically designed for a particular failure mechanism" such that the test structure is representative of the actual Al/TiN interconnect structure being investigated [MPEP 2144].

9. Claims 13-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamamoto as applied to claims 3 and 29 above, and further in view of Dreyer et al. (U.S. 5,049,811) taken with an excerpt from a 1965 text book (Integrated Circuit Design Principles, page 128, Figure 5-1).

Yamamoto is silent about the possible positioning of the "test device" runner.

Dreyer et al. teaches that a large multi-layer metal measurement structure (Fig. 5) "can be placed in the scribe grids or on individual die of a semiconductor wafer."

The 1965 textbook teaches that an area for circuit with bond pads at the periphery is old in the art, as clearly seen in Fig. 5-1.

It would have been obvious to one of ordinary skill in the art at the time of the claimed invention to include a test structure of Yamamoto in a wafer or streets (scribe grid) as is directed by Dreyer et al. when making known devices such as seen in Fig. 5-1. One of ordinary skill in the art would have been motivated to include a test structure to readily verify interconnect integrity [MPEP 2144].

It would have been obvious to one of ordinary skill in the art at the time of the claimed invention to include the test structure anywhere space is available that would experience representative process conditions, motivated for particular placement anywhere by the location of available space, such as at a corner of the die in Fig. 5-1, or in streets, such that the structure would be between bond pads and an edge of the die [MPEP 2144].

It would have been obvious to one of ordinary skill in the art to package working die having the test structure, motivated to sell the package.

It would have been obvious to have the bond pads at a higher level since the test structure of Yamamoto is multi-level and bond pads are made accessible at the top level.

10. Claims 34-41 (seemingly mischaracterized as "Invention II" per the withdrawn restriction requirement) are rejected under 35 U.S.C. 103(a) as being unpatentable over the reference(s) rejecting (apparently mischaracterized) "Invention I" (as defined by claims 1-33) since applicant has submitted that "only a single invention is present" among claims 1-41 (p. 2, paper 5).

Since "only a single invention is present," it would have been obvious to one of ordinary skill in the art at the time of the claimed invention to practice the method of claims 34-41 upon learning the "structure" defined by claims 1-33. The "method" (of claims 34-41) is not patentably distinct from the claimed "structure" (of claims 1-33), by applicant's own argument, so the claimed "structure" being anticipated/obvious must render the claimed "method" as anticipated/obvious (since "method" vs. "structure" = "single invention").

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

Ryan (U.S. Patent 5,930,587) is cited for teaching known mechanisms of interconnect voiding, including "stress migration" [col. 1]

Lee (U.S. Patent 5,872,018) is cited for teaching conductive runner test structures as "prior art" [Fig. 1, col. 2, lines 27-46 and col. 3, lines 10-54].

Matsunaga et al. (IEEE article) is cited for teaching stress-migration evaluation of Al/Ti/TiN interconnect configurations.

Hinode et al. (IEEE conference excerpt) is cited for teaching mechanisms of stress-induced voiding from interconnect migration.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Evan T. Pert whose telephone number is 703-306-5689. The examiner can normally be reached on M-F (7:00-3:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on 703-308-1233. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

EVAN PERT

ETP
February 21, 2003